Transformer-Coupled Converter for Voltage Modulation Techniques

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***Abstract*—In high performance digital systems as well as in RF systems, voltage scaling and modulation techniques have been adopted to achieve a more efficient processing of the energy. The implementation of such techniques relies on a power supply that is capable of rapidly adjusting the system supply voltage. In this paper, a pulsewidth modulation multiphase topology with magnetic coupling is proposed for its use in voltage modulation techniques. Since the magnetic coupling in this topology is done with transformers instead of coupled inductors, the energy storage is reduced and very fast voltage changes are achieved. Advantages and drawbacks of this topology have been previously presented in the literature and in this paper, the design criteria for implementing a power supply for the envelope elimination and restoration technique in an RF system are presented along with an implementation of the power supply.**

***Index Terms*—Envelope elimination and restoration (EER) technique, multiphase coupled converter, no energy storage, RF power amplifier, voltage modulation.**

I. Introduction: Voltage Modulation Technique

MORE efficient processing of the energy has been a matter of interest in many fields of power electronics since energy savings reflect directly in cost savings and higher autonomy of mobile devices. For instance, communication and digital systems are two applications where a more efficient processing of the energy means higher autonomy of mobile devices. Techniques such as dynamic voltage scaling (DVS) are employed in order to reduce the power consumption of high-performance digital systems while in RF systems, techniques such as envelope elimination and restoration (EER) and envelope tracking (ET) are employed. In these techniques, the power supply plays an important role, since the energy savings rely partly on the power supply ability to rapidly adjust the output voltage. Besides adequately adjusting the output voltage, power supplies must accomplish other requirements in order to enable voltage modulation. Some of these requirements are the following ([1], [2]):

1) small size;
2) fast dynamic response (voltage and current steps);
3) high efficiency over a wide load range;
4) power supplies for RF systems should also ensure not to interfere with the output spectrum of the transmitter and to exhibit good tracking fidelity;
5) in DVS applications, it is also important for the power supply to exhibit very good static regulation.

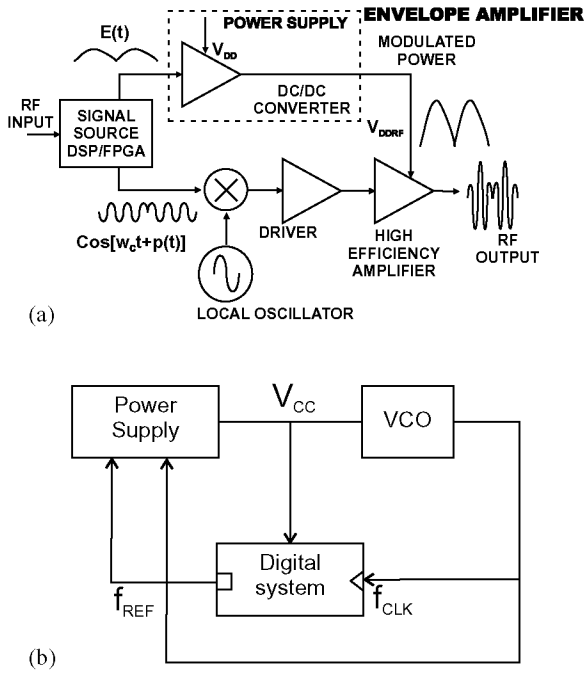


Fig. 1. (a) Simplified scheme of a power amplifier based on the EER technique: highly efficient power supply of the nonlinear power amplifier must produce a modulated output voltage in order to inject the envelope modulation. (b) System architecture for DVS implementation [1]. In both systems, adjusting the power supply output can lead to a more efficient processing of the energy.

A simplified block diagram of both a digital system with DVS architecture and a power amplifier that uses the EER technique are shown in Fig. 1. In this technique, the power supply modulating the supply voltage of the nonlinear RF PA is usually denominated as an envelope amplifier. In the case of the DVS technique, the power supply has to adjust the output voltage depending on the needs of the microprocessor and in that way significant power savings can be obtained in comparison when the microprocessor is supplied by constant voltage. When the

ET technique is applied, the power supply (the envelope amplifier) has a similar task; it has to supply a linear power amplifier with just enough voltage, avoiding clipping of the output signal. On the other hand, when a power supply is used in the EER technique, it has to modulate the power supply of the nonlinear power amplifier in order to inject the necessary envelope modulation into the output signal. Although these two techniques (ET and EER) are very similar (in both techniques the high efficiency of the envelope amplifier is extremely important), the demanded tracking fidelity of the power supply in the case of EER is significantly higher. This is due to the fact that the bandwidth of the envelope amplifier is directly responsible for the linearity of the complete RF PA in the case of EER. In [3], it has been shown that the minimum bandwidth of the envelope amplifier should be 3–5 times higher than the bandwidth of the transmitted RF signal in order to obtain good levels of linearity. On the other hand, the envelope amplifier for ET does not have to reproduce exact replica of the envelope amplifier and the linearity of the RF PA depends on the employed transistor in the linear regulator as it can be seen in [4]. Different power supplies for the implementation of voltage modulation techniques have been proposed in the literature, these solutions comprise pulsewidth modulation (PWM) topologies as in [1] and [5], multilevel converters, as in [2] or hybrid solutions that employ linear regulators [6].

The main drawbacks of using a PWM converter for this kind of applications rely on the complexity of the design of the output filter and the control [7]. The output filter should have an adequate size in order to accomplish certain requirements of current and voltage ripple but should also allow very fast changes in the output voltage level, requirements that can be considered contradictory. A converter operating at very high switching frequency (megahertz range) is necessary, along with a very fast control loop. These requirements increase the complexity of the PWM power supply. In the case of EER, if the transmitted signal has a bandwidth of 1MHz, the envelope amplifier should have the bandwidth of, at least, 4 MHz which leads to a switching frequency between 28 MHz and 36 MHz.

In this paper, a PWM multiphase topology that could avoid some of these drawbacks is proposed to be used for supply voltage modulation in RF power amplifiers. This topology is previously presented in [8] along with its operating principle and design guidelines. In the following sections, the operating principle of the topology is briefly reviewed and the design of a four-phase converter optimized for tracking an envelope amplifier and for achieving fast voltage steps is presented.

The "transformer-coupled converter," presented in [8] is based on a multiphase converter with magnetic coupling among the phases. In the proposed converter, the phases are coupled with transformers instead of coupled inductors [9]. Since transformers are, ideally, no energy storing devices, the energy storage in the converter is minimized. Ideally, the energy transfer from the input and to the output is instantaneous, so the output voltage can be changed with a very high slew rate.

An implementation of the EER technique proposed in the literature [2] is used to prove the feasibility of the "transformer-coupled converter" as voltage supply modulator. The EER implementation proposed in [2] is shown in Fig. 2 and in this

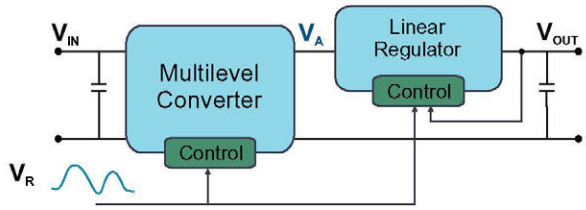


Fig. 2. Simplified schematic of the envelope amplifier proposed in [2], the multilevel converter should show high efficiency and accomplish fast voltage steps in order to supply the linear regulator with an adequate voltage.

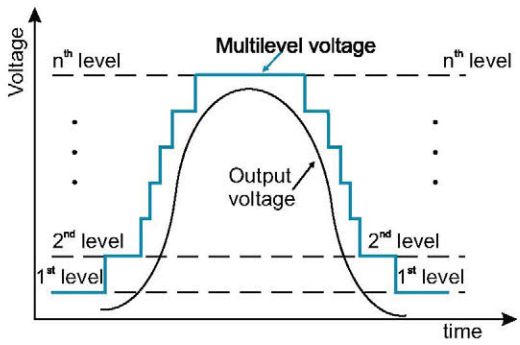


Fig. 3. Waveforms of the proposed envelope amplifier.

solution a fast multilevel converter is used in series with a linear regulator in order to exploit all good dynamic characteristics of the linear regulator regarding its bandwidth and linearity. By employing a multilevel converter as the voltage supply of the linear regulator and by adjusting its output voltage depending on the level of the reconstructed envelope, it is possible to obtain significant energy savings. This concept is illustrated with the waveforms shown in Fig. 3. The topology proposed in [8] can be used as a multilevel converter to provide an output voltage with a discrete number of outputs for the architecture proposed in [2] and illustrated in Fig. 2, this is explained in detail in Section III. An experimental prototype developed for this solution and the complete system setup are presented in Section IV.

II. Transformer-Coupled Converter: Review of Operating Principle and Features

As mentioned earlier, when using PWM converters for voltage modulation techniques, such as EER, one of the main drawbacks is the design of the feedback and the output filter [7], [10]. This design is a direct tradeoff between the achievable bandwidth of the converter and the filtering of the output ripple [1].

Tight filtering needs can be easily met with a high value of inductor that allows the reduction of the current ripple. However, the energy stored in this inductor will limit the energy transfer when a load change or voltage step is demanded to the converter. Increasing the switching frequency allows using a small inductor and capacitor values, while accomplishing tight filtering and enough bandwidth. The main drawback when rising operating frequency of power converters is that switching losses also increase, degrading the efficiency of the converter and hence the overall efficiency of the system where the power

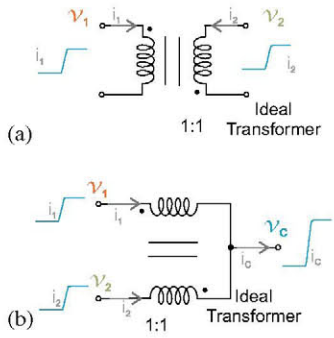


Fig. 4. Current step that occurs in the secondary winding of an ideal transformer will be immediately reflected in the primary winding of the transformer.

supply is placed. In order to find a better tradeoff among dynamic response, filtering and efficiency, multiphase converters were proposed in the literature [11]. Thanks to current ripple cancellation in multiphase converters, smaller inductance values can be used, while still accomplishing filtering needs.

A. *Operating Principle*

The topology proposed in [8] can be described as a multiphase converter with magnetic coupling among the phases; however, the phases of the proposed converter are coupled using discrete transformers instead of coupled inductors. Transformers are ideally no energy storing elements, a current step applied to the secondary of the transformer will be immediately reflected in the primary as shown in Fig. 4.

The objective of using transformers as coupling elements is to reduce the energy stored in series between the input and the output of the converter. A transformer can be used in a multiphase converter if connected as shown in Fig. 4. The ideal transformer shown in Fig. 4(a) can be used as shown in Fig. 4(b), where v_1 and v_2 are the voltages applied to the input terminals of the transformer and v_c is the voltage at the output terminal

$$v_1 - v_c = v_c - v_2 \tag{1}$$

hence

$$v_c = \frac{v_1 + v_2}{2}. \tag{2}$$

If certain duty cycles are applied, a constant output voltage can be obtained; for example, in Fig. 5, basic operating waveforms for 50% duty cycle are shown. For 50% duty cycle, following two conditions are accomplished:

1) The sum of the voltages at the input of the transformer $\sum v_i$ *is constant for every instant* along a switching cycle. In Fig. 5, $v_1 + v_2 = \text{constant}\ \forall t$.
2) The mean voltage value $\bar{v}_i$ applied to each input of the transformer must be equal in order to avoid transformer saturation. In Fig. 5, $\bar{v_1} = \bar{v_2} = v_c$. The mean value of the voltage across the transformer is zero.

These conditions can be accomplished only at certain duty cycles. At the duty cycles where these conditions are accomplished, output voltage of the topology is kept constant; outside

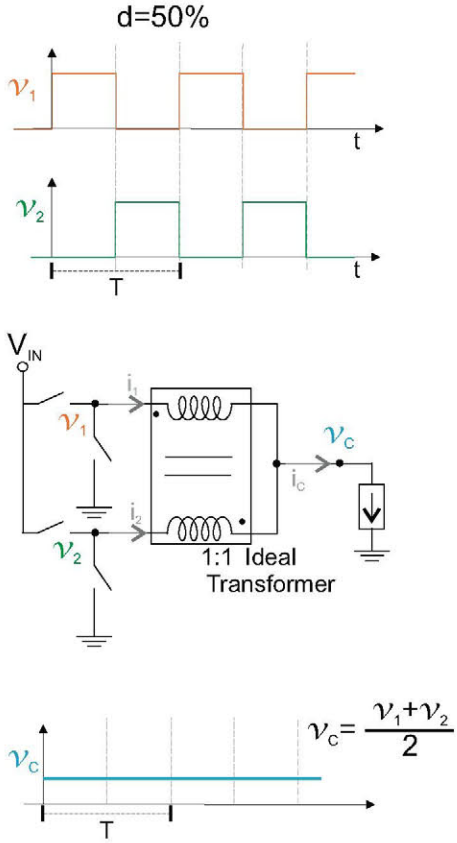


Fig. 5. Basic waveforms and schematic of a two-phase transformer-coupled topology, if the sum of the input voltages to the transformer for every instant along a switching cycle is constant, the output filter is not needed.

these allowed duty cycles, a pulsating voltage with an amplitude equal to $\frac{v_1+v_2}{2}$ appears at the output voltage since no output filter is placed, this is shown in Fig. 6.

In a four-phase converter, constant output voltages are accomplished for 0%, 25%, 50%, 75%, and 100% duty cycles. A four-phase converter built with discrete transformers is illustrated in Fig. 7(c). In Fig. 7(a) and (b), waveforms for 25% and 50% duty cycles are illustrated, respectively.

With 25% duty cycle [see Fig. 7(a)], there is one active phase connected to V_{IN} for every instant of time.

1) During t_0–t_1, phase 1 is connected to V_{IN} and transfers energy from the input to the set of transformers, while the other phases are connected to ground. During this instant of time, the sum of the input voltages to the set of transformers is given by

$$v_1 + v_2 + v_3 + v_4 = V_{\text{IN}}.$$

2) At t_1, phase 1 changes from V_{IN} to ground, and at the same time, phase 2 changes from ground to V_{IN}, since the energy flow must remain constant for every instant of time.
3) During t_1–t_2, phase 2 is connected to V_{IN}, making v_2 equal to V_{IN}. The rest of the phases are connected to ground so that $v_1 + v_2 + v_3 + v_4 = V_{\text{IN}}$ is also accomplished for this instant of time.

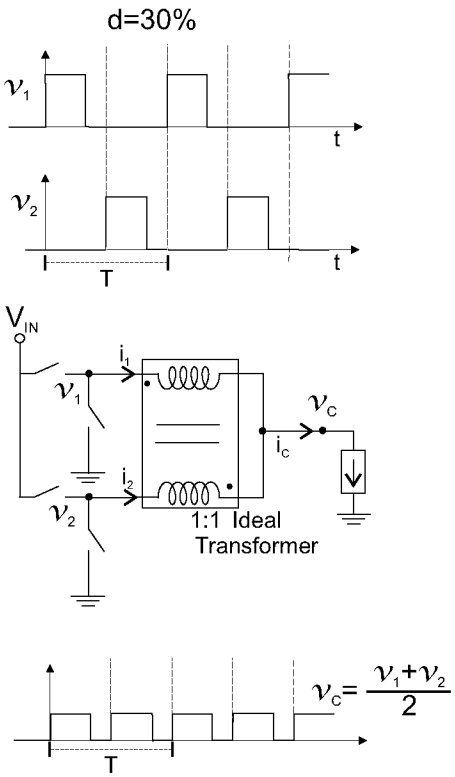


Fig. 6. At the duty cycles where the sum of $v_1 + v_2$ is not constant along a switching cycle, a pulsating voltage appears at the output since there is no output filter.

The same process is repeated for phases 3 and 4 during t_2–t_3 and t_3–t_4. Table I summarizes the values of the input voltages to the set of transformers for every instant of time, and Table II shows the value of the voltages of each transformer ($T1$, $T2$, $T3$, and $T4$, see Fig. 7) for the same instants of time.

The sum of the voltages at the inputs of the set of transformers $v_1 + v_2 + v_3 + v_4$ is constant and equal to $1 \cdot V_{\mathrm{IN}}$ for every instant of time; hence, mean voltage value of all phases along a switching cycle is given by

$$\bar{v_i} = \frac{v_1 + v_2 + v_3 + v_4}{4} = \frac{1 \cdot V_{\mathrm{IN}}}{4}. \tag{3}$$

At the output of the set of transformers, a constant output voltage V_{OUT} equal to $\frac{V_{\mathrm{IN}}}{4}$ is obtained.

For 50% duty cycle, two phases are connected to V_{IN} for every instant of time; hence, the sum of the voltages at the inputs of the set of transformers $v_1 + v_2 + v_3 + v_4$ is constant and equal to $2 \cdot V_{\mathrm{IN}}$ for every instant of time; mean voltage values of all phases along a switching cycle are equal and given by

$$\bar{v_1} = \bar{v_2} = \bar{v_3} = \bar{v_4} = \frac{2 \cdot V_{\mathrm{IN}}}{4}. \tag{4}$$

At the output of the set of transformers, a constant output voltage V_{OUT} equal to $\frac{V_{\mathrm{IN}}}{2}$ is obtained.

When the duty cycle is equal to 75% there are three phases transferring energy to the magnetic structure for every instant of time and the mean voltage value of the phases is given by

$$\bar{v_1} = \bar{v_2} = \bar{v_3} = \bar{v_4} = \frac{3 \cdot V_{\mathrm{IN}}}{4}. \tag{5}$$

For these duty cycles 25%, 50%, and 75%, the output voltage of the set of transformers V_{OUT} remains constant for every instant of time and ideally, it is not necessary to place an output filter.

Without the output inductor, only the equivalent leakage inductance of the set of transformers and the stray inductance of the printed circuit board (PCB) are found in series between the input and the output of the converter. The value of the leakage inductance can be minimized (to tenths of nanohenry) if the adequate interleaving technique is used [12] hence minimizing the energy storage in the converter.

Detailed operation of this converter and generalization of the concept are reported in [8]; the operation of a four-phase converter with minimum energy storage has been briefly reviewed since the application proposed in this paper is based on a four-phase transformer-coupled converter. The load of the transformer-coupled converter is represented with a current source for simplicity and because it is a good approximation for the linear regulator connected to the converter in the final implementation; however, in a general case it can be purely resistive as well.

B. Features of Transformer-Coupled Converter

1) *Dynamic response*. If no inductor is placed in series between the input and output of the converter, the predominant dynamic response during a load step is determined by the transformer; only the equivalent leakage inductance of the transformers will slow down the dynamic response of the converter.
2) *Switching frequency is a design degree of freedom*. Since there is, ideally, no energy stored in the converter, the switching frequency does not affect the dynamic response of the topology. The frequency can be chosen to design a converter with reduced size or to favor the efficiency.
3) *Discrete output voltage values*. Since there is no energy storage in the transformer-coupled converter, the regulation capability of the topology is lost; only certain values can be obtained and fast changes between this discrete values are possible. If the duty cycle is modulated with a certain waveform, the converter will follow this waveform within discrete values, as shown in Fig. 8.
4) *Current sharing*. The current sharing among the phases is assessed by the operation of the topology since the ampere-turns balance of the transformers should be accomplished.
5) *Equivalent series inductance*. In the implementation of an actual converter, energy is stored in the leakage inductance of the transformers and the stray inductance of the PCB. The equivalent leakage inductance of the transformers is obtained as shown in Fig. 9. With equal turns number in the primary and in the secondary ($N_1 = N_2$), as explained in [13], the measured leakage inductance can be split

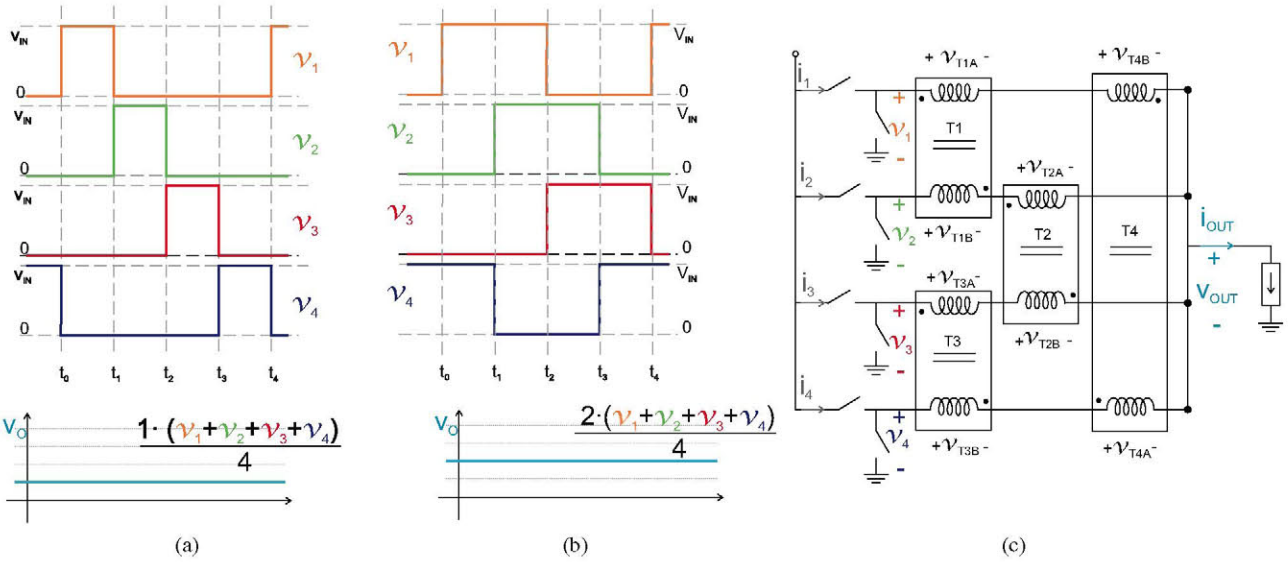


Fig. 7. (a) Operating waveforms for transformer-coupled converter when $d = 25\%$ the sum of this waveforms results in a constant voltage for every instant of time. (b) Operating voltage waveforms for $d = 50\%$. (c) Schematic diagram of proposed topology with four phases.

TABLE I
PHASE VOLTAGES (SEE FIG. 7) FOR THE DIFFERENT TIME INTERVALS WITH 25% DUTY CYCLE, FOR EVERY INSTANT OF TIME $v_1 + v_2 + v_3 + v_4 = V_{IN}$

Time Interval	v_1	v_2	v_3	v_4
$t_0 - t_1$	V_{IN}	0	0	0
$t_1 - t_2$	0	V_{IN}	0	0
$t_2 - t_3$	0	0	V_{IN}	0
$t_3 - t_4$	0	0	0	V_{IN}

TABLE II
TRANSFORMER VOLTAGE VALUES FOR T_1, T_2, T_3, AND T_4 FOR 25% DUTY CYCLE

Time Interval	v_{T1A}	v_{T2A}	v_{T3A}	v_{T4A}
$t_0 - t_1$	$\frac{3}{8}\cdot V_{IN}$	$\frac{1}{8}\cdot V_{IN}$	$-\frac{1}{8}\cdot V_{IN}$	$-\frac{3}{8}\cdot V_{IN}$
$t_1 - t_2$	$-\frac{1}{8}\cdot V_{IN}$	$\frac{3}{8}\cdot V_{IN}$	$\frac{3}{8}\cdot V_{IN}$	$-\frac{1}{8}\cdot V_{IN}$
$t_2 - t_3$	$-\frac{3}{8}\cdot V_{IN}$	$-\frac{1}{8}\cdot V_{IN}$	$\frac{1}{8}\cdot V_{IN}$	$\frac{3}{8}\cdot V_{IN}$
$t_3 - t_4$	$\frac{1}{8}\cdot V_{IN}$	$-\frac{3}{8}\cdot V_{IN}$	$-\frac{3}{8}\cdot V_{IN}$	$\frac{1}{8}\cdot V_{IN}$

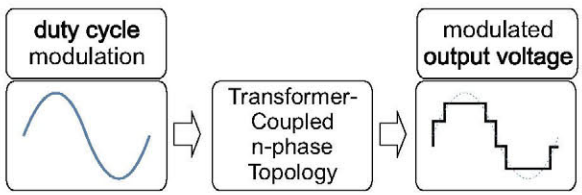


Fig. 8. Output voltage of the proposed topology can be changed only within discrete values.

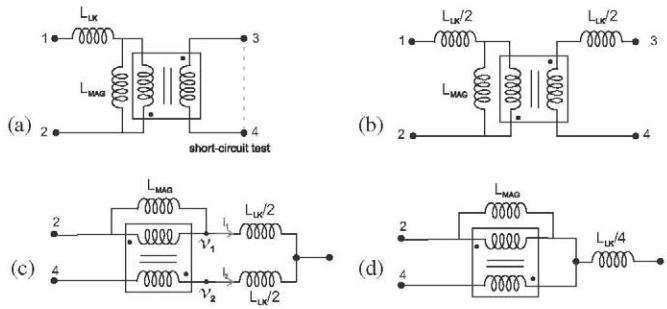


Fig. 9. Equivalent series inductance in the proposed topology is formed by the leakage inductance of the transformer(s) and by the stray inductance of the prototype. Equivalent leakage inductance of the transformers is obtained as shown [13], (a), (b), and (c) are equivalent; (c) is equivalent with (d) since $i_1 = i_2$.

symmetrically in half and placed in series with each winding. Also, the implementation of the transformer is done as symmetrical as possible; an axial view of the implementation of the transformer is shown in Fig. 18.

III. DESIGN CRITERIA

As explained in the last section, the proposed topology achieves high-efficiency energy conversion with minimum energy storage. With minimum energy storage, fast energy transfer between the input and the output of the converter is enabled even at low switching frequencies. Due to these advantages, the transformer-coupled topology can be considered a good candidate to be used in RF architectures where a fast modulation of the supply voltage is needed such as EER or ET. Besides these two previously described techniques, there are other RF systems that could benefit from the modulation of the power supply. Some of the possible architectures which could benefit from this solution are class G power amplifier [14], multilevel LINC [15], and assymetric multilevel outphasing systems [16].

The implementation of EER technique proposed in [2] is shown in Fig. 10; this solution is formed by a multioutput dc–dc converter, a multilevel converter, and a linear regulator. The task of both the multioutput converter and the multilevel converter is to provide the linear regulator with a supply voltage that is close to the linear regulator output voltage, the power losses in the linear regulator will be reduced and the overall system efficiency can be increased. The supply voltage of the linear

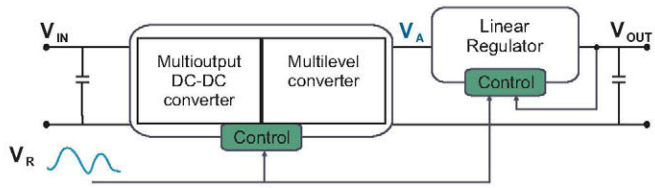


Fig. 10. Both the multioutput and the multilevel converters adjust the supply voltage of the linear regulator. This solution is proposed in [2] to increase the efficiency of the envelope amplifier in the RF systems.

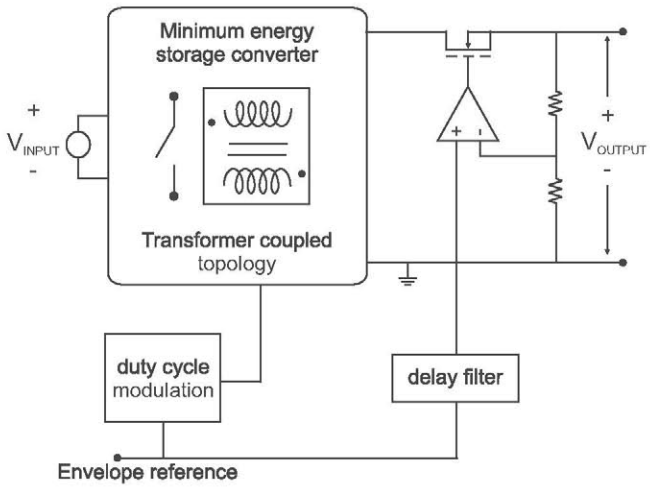


Fig. 11. Complete system setup with the transformer-coupled converter topology. The linear regulator filters the noise from the multiphase converter.

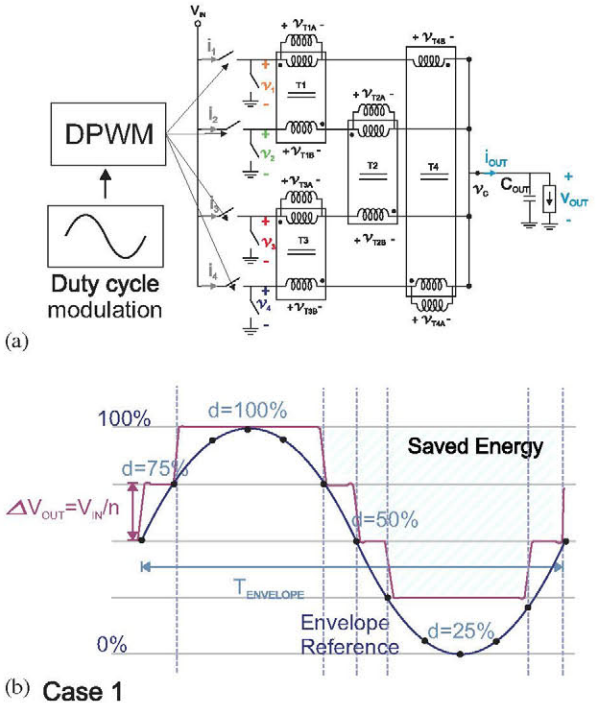


Fig. 12. (a) Sinusoidal reference is used to modulate the duty cycle applied to the converter, the resulting output voltage follows the sinusoidal reference within discrete steps. (b) Sinusoidal reference followed with four levels.

regulator should always be higher than its output voltage in order to ensure correct operation.

In Fig. 11, the transformer-coupled converter is proposed to be used both as the multioutput and the multilevel converter in the envelope amplifier. If the envelope reference is used to modulate the duty cycle of the transformer-coupled converter, the output voltage of the topology will follow this reference within discrete steps. For this reason, this topology can be considered as a power analog to digital converter; in Figs. 12 and 13, the output voltage of a four-phase converter where the duty cycle is modulated with a sinusoidal waveform is shown.

In Fig. 12, a small output capacitor is included because in the real converter, there are several nonidealities (time delays, series resistance, and series inductance [8]) that cause slight oscillations in the output voltage of the converter; hence, it is necessary to place a small capacitor (C_{OUT} in Fig. 12) to reduce the high-frequency ripple.

The transient response of the topology can be modeled with the circuit shown in Fig. 14, since the energy stored in the converter is minimized, the dynamic response of the converter is independent from the switching frequency and the input and output impedances of the converter are the elements that mainly define the dynamic response of the converter. Z_{BUS} is the intermediate impedance of the converter and it is formed by the output impedance of the input source V_{IN} and the impedance of the connection cables. $Z_{C\mathrm{IN}}$ is the impedance of the input capacitor C_{IN} including its parasitics. The series impedance Z_{SERIES} is formed by the dc equivalent series resistance R_{SERIES} and the series inductance L_{SERIES}. The output capacitor is also considered along with its parasitic ESL and ESR and it is named $Z_{C\mathrm{OUT}}$ impedance.

The inductance L_{SERIES} is formed by the equivalent leakage inductance of the transformers arrangement (obtained as shown in Fig. 9) plus the PCB stray inductance. Low leakage inductance values of the transformers can be obtained if the adequate construction technology is used [12], [17] and values as low as tenths of nanohenry can be achieved. L_{SERIES} represents the energy stored between the input and the output of the converter.

From this model, the maximum achievable dv/dt can be obtained; for example, for $L_{\mathrm{SERIES}} = 30\,\mathrm{nH}$ and $C_{\mathrm{OUT}} = 1\,\mathrm{nF}$, dv/dt is theoretically 470 $\mathrm{V}/\mu\mathrm{s}$.

Since the transient response of the converter is mainly defined by the input and output impedances of the converter (Z_{BUS} and Z_{OUT} in Fig. 14), the operating frequency of the converter can be determined independently from the dynamic response but taking into account the envelope reference to be tracked.

The switching frequency of the converter should be chosen according to the dynamic of the envelope reference and taking into account that the output voltage of the multilevel converter must be higher than the voltage of the desired envelope at every instant. It is possible that a change in the output voltage of the multilevel converter is triggered by one sample of the envelope and that one sample period later a change in the output voltage is triggered again; this is illustrated in Fig. 15. From this figure, it can be seen that the multilevel converter can achieve the

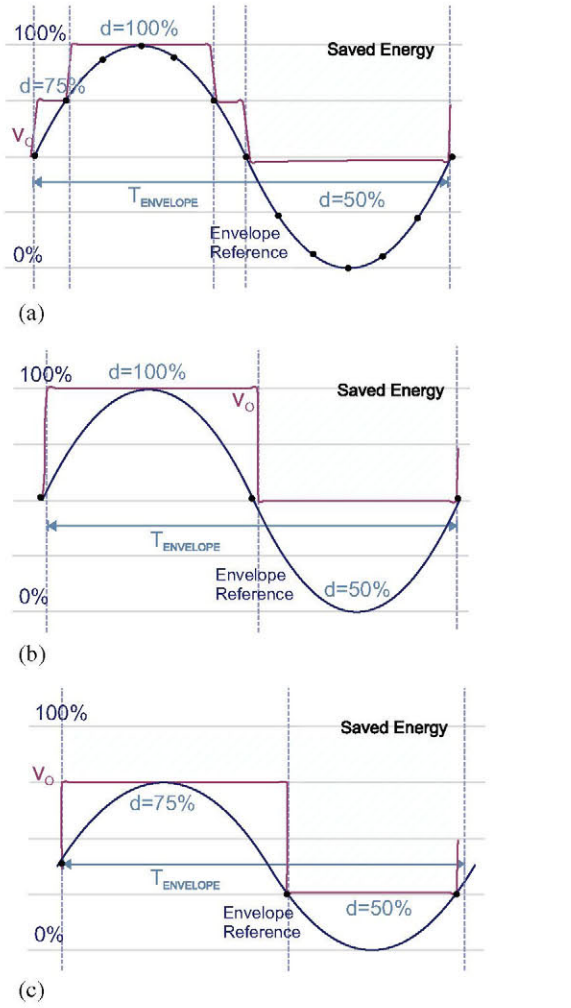


Fig. 13. (a) Sinusoidal waveform (envelope reference) followed with three levels. (b) and (c) are two examples of sinusoidal waveforms followed with low resolution (two levels). The shaded areas represent the saved energy.

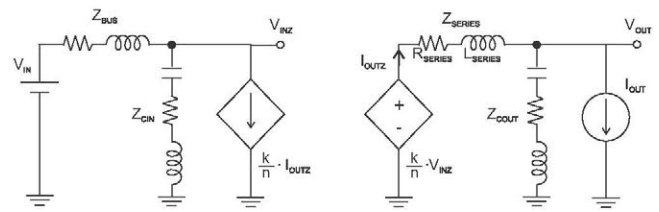


Fig. 14. Large signal model for calculating the maximum dv/dt of the "minimum energy storage" topology. L_{SERIES}, R_{SERIES} can be measured from the prototype.

voltage changes as fast as necessary only if the switching frequency of the converter is equal to the sampling frequency of the envelope.

Therefore, if the sampling frequency is N_S times higher than the bandwidth of the envelope ($\mathrm{BW}_{\mathrm{envelope}}$), the switching frequency of the converter can be chosen according to

$$f_{\mathrm{SW}} = N_S \cdot \mathrm{BW}_{\mathrm{envelope}} \tag{6}$$

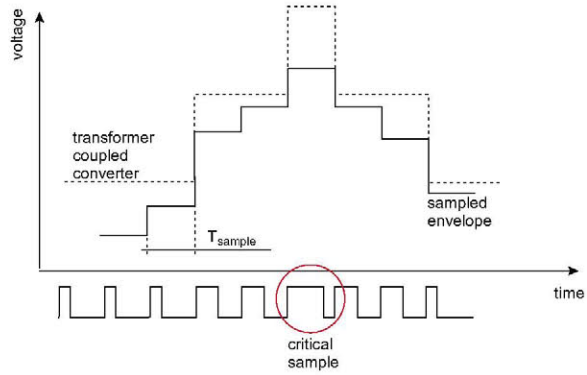


Fig. 15. High switching frequency is needed in the transformer coupled converter in order to track an envelope reference with fast changes.

and the sampling frequency of the envelope N_S can be 10–20 times higher than its bandwidth, depending on the levels of the quantization noise, for example.

This can be illustrated with the sinusoidal reference shown in Fig. 12. Sampling ratio N is set to 14 and the bandwidth is equal to the frequency of the sinusoidal envelope reference, 150 kHz for this example. The envelope reference is followed with four voltage levels and the duty cycle of the converter is set as follows:

1) $d = 100\%$ when the amplitude of the sinusoidal waveform is higher than 75%;
2) $d = 75\%$ when the amplitude of the sinusoidal waveform (envelope reference) is between 50% and 75%;
3) $d = 50\%$ when the amplitude of the sinusoidal waveform is between 25% and 50%;
4) $d = 25\%$ when the amplitude of the sinusoidal waveform is smaller than 25%.

With the frequency of the envelope reference equal to 150 kHz and the sampling ratio equal to 14 samples, the switching frequency of the converter is given by (6) and equal to 1.8 MHz.

A similar criteria for following the envelope reference is shown in Fig. 13(a). The envelope reference is followed with the same resolution but using only three supply voltage levels. The same switching frequency (1.8 MHz) would be necessary if the sampling ratio is the same ($N = 14$), and the frequency of the sinusoidal waveform is the same (150 kHz), hence the relation between the switching frequency of the converter and the envelope reference is independent from the number of voltage levels used for tracking the envelope reference.

To modify the relation between the switching frequency of the converter and the bandwidth of the envelope reference, a different sampling ratio can be adopted.

If the signals are known in advance, the sampling ratio can be reduced and higher frequency signals can be tracked with the same converter. For example, in Fig. 13(b) and (c), the sampling ratio N_S has been reduced to 2, with this sampling ratio, an envelope amplifier with a higher frequency can be followed; for example a sinusoidal envelope of 1 MHz bandwidth can be tracked with the same 2 MHz switching frequency converter. In this case, the envelope amplifier is tracked with lower resolution. This could reduce the energy savings but also the switching

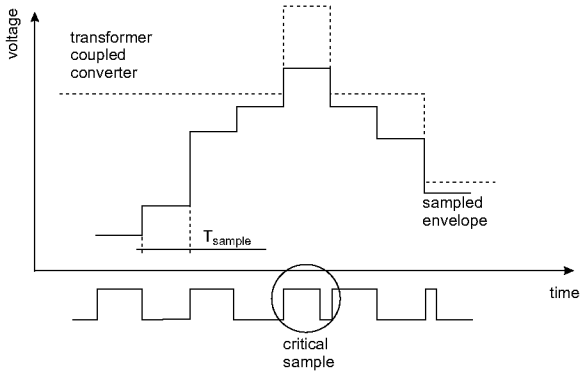


Fig. 16. If the envelope reference is known in advance, the switching frequency of the transformer-coupled converter can be reduced.

losses of the dc/dc converter can be reduced; also, in Fig. 13(c), a sinusoidal envelope reference with a different amplitude is presented, the criteria of $N_S = 2$ can be also applied in this case.

In the case of a random signal, it is more difficult to achieve a reduction in the switching frequency of the converter. If the signal is tracked with a low number of levels (for example, two), the same voltage level could be applied during consecutive samples due to the high peak-to-average power ratio (PAPR) property of the signals. During this period of time, the switching frequency can be decreased in order to reduce switching losses in the converter. However, the switching frequency should be increased again if fast voltage changes are required again. This approach is illustrated in Fig. 16. In order to implement this approach, it would be necessary to analyze the envelope reference in real time ("on the fly") which could complicate the design and the implementation. In this paper, the multilevel converter is implemented using constant switching frequency.

Although sinusoidal waveforms are regularly used as the envelope reference to analyze RF systems, it is true that the real envelope amplifier is a sum of different harmonics and amplitudes; therefore, in Figs. 12(b) and 13(a)–(c), different sinusoidal waveforms tracked with different number of levels and different sampling ratios are shown. In each figure, the shaded area stands for the energy that is saved (over one envelope reference cycle) when compared to an envelope amplifier with fixed supply voltage; the higher the number of levels, the higher the amount of saved energy. A study of the efficiency of the envelope amplifier with different voltage levels is presented in [2]. In Table III, a summary of the losses for the sinusoidal envelope references of Figs. 12(b) and 13(a)–(c) is presented. For the same sinusoidal reference (cases 1, 2, and 3), a higher amount of energy is saved when the resolution for following the envelope is higher. On the other hand, for a waveform with an amplitude of 75% (Case 4) a significant amount of power is saved even when the envelope amplifier is followed with low resolution. The amount of saved power is calculated as in [2].

The power that is saved for each case is different depending on the amplitude of the envelope reference (see Table III); since an actual envelope reference is formed by the sum of waveforms with different amplitudes and frequencies, the average saved power depends on the real transmitted signal. If the average amplitude of the signal is medium (which is typical in RF amplifiers [2]), the average saved power would be higher (for example, case 4 in Table III).

To estimate the overall efficiency of the envelope amplifier when a 64QAM signal is reproduced, it is necessary to do an analysis on how the efficiency of the envelope amplifier is changed with different number of voltage levels. In order to do this analysis, an adequate model of the transformer-coupled converter is necessary.

The power losses of the transformer-coupled converter can be modeled in the same way than in a four-phase buck converter, assuming ideal current sharing and zero current ripple. The efficiency of a single phase is modeled using the model explained in [18]. In this model, the transistors are replaced with nonlinear capacitors, variable current sources, and resistances, depending on which moment of the switching transient is being modeled. The parameter of the transistors (capacitances, transconductances, etc.) is obtained from the datasheet. The influence of the dead times, the output impedance of the driver, and the parasitic inductances of the package have been taken into account as well. The comparison between the measurement and the calculation of the efficiency are shown in Fig. 17. The MOSFETs are IRF8915 and the drivers LM27222.

For the static measurements, the accuracy of the model is very high; however, it is necessary to calculate the efficiency of the overall system in the case of a random signal. The envelope of an RF signal is usually described with its probability density function, $p(V_{\text{envelope}})$. This information must be used in order to estimate the efficiency of the envelope amplifier.

For the given value of the envelope, it is possible to estimate the power losses of the envelope amplifier quite accurately using the aforementioned power losses model and taking into account the fact that the efficiency of the linear regulator is equal to the ratio of its output and supply voltage. In order to calculate the average power losses, the static power losses should be averaged as follows:

$$P_{EA}\ \text{average losses} = \int_0^{V_{\max}} P_{EA\ \text{static losses}}(v_{\text{envelope}})p(v_{\text{envelope}})d(v_{\text{envelope}}) \tag{7}$$

$$P_{EA\ \text{static losses}}(v_{\text{envelope}}) = P_{\text{transformer coupled}}(v_{\text{transformer coupled}}) + \frac{v_{\text{transformer coupled}} - v_{\text{envelope}}}{R_{\text{load}}} v_{\text{envelope}} \tag{8}$$

where V_{MAX} is the maximum level of the envelope, $P_{EA\ \text{static losses}}$ are the power losses of the envelope amplifier for the given envelope level, p is the probability density function of the envelope, $V_{\text{transformer coupled}}$ is the output of the transformer-coupled converter that depends on the number of the phases and the instantaneous envelope level and R_{load} is the load.

TABLE III
AMOUNT OF POWER SAVED FOR DIFFERENT SINUSOIDAL ENVELOPE REFERENCES ASSUMING NO LOSSES IN THE VOLTAGE SUPPLY MODULATOR CONVERTER

	power losses WITHOUT modulation	envelope amplitude	# of levels	power losses with modulation	Saved Power
Case 1 (Fig. 12b)	$33\% \cdot P_{OUT}$	100%	4	$12\% \cdot P_{OUT}$	$21\% \cdot P_{OUT}$
Case 2 (Fig. 13a)	$33\% \cdot P_{OUT}$	100%	3	$14\% \cdot P_{OUT}$	$19\% \cdot P_{OUT}$
Case 3 (Fig. 13b)	$33\% \cdot P_{OUT}$	100%	2	$21\% \cdot P_{OUT}$	$12\% \cdot P_{OUT}$
Case 4 (Fig. 13c)	$79\% \cdot P_{OUT}$	75%	2	$20\% \cdot P_{OUT}$	$59\% \cdot P_{OUT}$

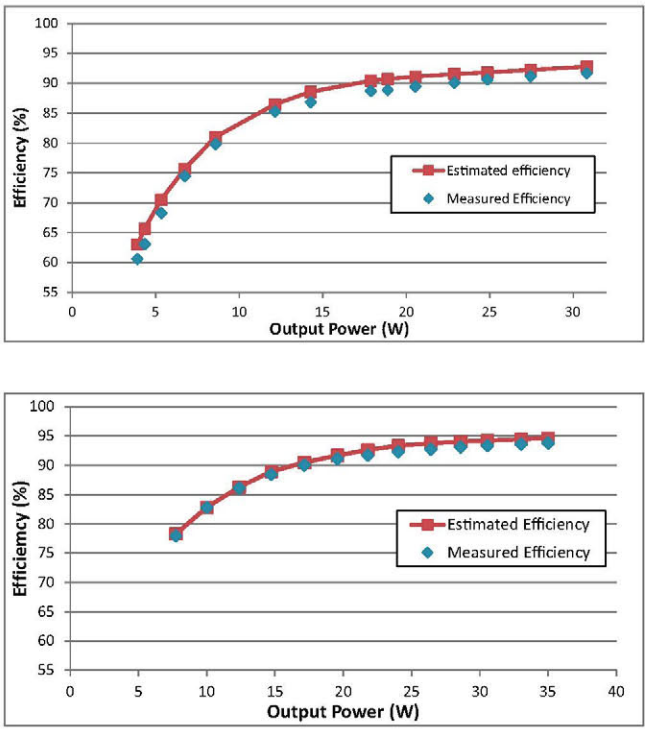


Fig. 17. Power losses model reported in [18] is used to calculate the efficiency of the transformer-coupled converter.

Using previous equations, the overall efficiency is calculated as follows:

$$\eta = \frac{\int_0^{V_{\max}} \frac{v_{\text{envelope}}^2}{R_{\text{load}}} p(v_{\text{envelope}}) dv_{\text{envelope}}}{P_{EA\ \text{average losses}} + \int_0^{V_{\max}} \frac{v_{\text{envelope}}^2}{R_{\text{load}}} p(v_{\text{envelope}}) dv_{\text{envelope}}}. \quad (9)$$

Using this equation, the efficiency is calculated for different setups; the number of levels and the voltage distribution is changed. A test signal of the following characteristics is considered: 200 kHz 64QAM signal with a maximum amplitude of 16 V, average output power is around 10.5 W, and the peak power is around 50 W. A relevant time diagram of the linear regulator and the transformer-coupled converter along with the details of the implementation is given in Section IV.

In Table IV, the calculations of the efficiency for different number of voltage levels are given. In order to confirm the accuracy of the calculations, two measurements (for the cases of three and four levels) are also included. In the column "voltage distribution" the voltage levels that are used to track the envelope reference are shown; since the input voltage is 17 V, these levels are 4.25 V, 8.5 V, 12.75 V, and 17V for the 0.25 Vmax/0.5 Vmax/.75 Vmax/1 Vmax case. In the column "phases needed," the number of phases to implement these duty cycles is shown.

Two conclusions can be obtained from this table. First, the calculations are in agreement with the measurements; the difference between the calculated and the measured efficiency is smaller than 1%. Second, the efficiency of the overall envelope amplifier is increased when the number of levels is also increased, until the optimum number of levels is reached and then the efficiency decreases.

To determine the optimum number of levels, the efficiency of the transformer-coupled converter and the linear regulator should be analyzed separately. In the linear regulator, the efficiency increases with the number of levels, and also, the efficiency changes if the voltage distribution is changed; in Table IV, for the same number of levels (three levels), a higher efficiency for the linear regulator is attained with nonequidistant voltage levels (0.5 Vmax/0.75 Vmax/Vmax) when compared to equidistant voltage levels (0.33 Vmax/0.67 Vmax/Vmax). In the transformer coupled converter, the efficiency depends on the number of phases. The results shown in Table IV are obtained with the same MOSFET in all the setups, independently from the power processed per phase. When more phases are used, a lower amount of power is processed by each phase and with lower processed power per phase the efficiency drops down, as shown in Fig. 17. If a more adequate MOSFET (less parasitic capacitances and higher on-resistance) is selected for higher number of phases, the efficiency could remain high. In any case, a high number of phases/high number of voltage levels would require a higher switching frequency to apply all the voltage levels, lowering the efficiency of the transformer-coupled converter. For a given specifications and using this losses model, the optimum number of phases can be determined. The distribution of voltage levels also impacts the efficiency of the transformer-coupled converter. In [2], it has been explained that the equidistant voltage distribution (0.33 Vmax/0.67 Vmax/Vmax) does not have to be the optimal one. However, in this implementation, higher efficiency is attained with equidistant voltage levels. Due to the features of the transformer-coupled converter, only three phases are required to implement three equidistant voltage levels but four phases are required to implement three nonequidistant voltage levels. In this last case, more magnetic components are required and less energy per phase is handled.

The efficiency of the linear regulator is higher if it is supplied with voltage levels that are relatively high (for example, 0.5 Vmax/0.75 Vmax/Vmax) due to the nonuniform distribution of the envelope and its high PAPR property. This is due to the fact that the highest power losses of the linear regulator are at high envelope levels (due to high currents of the load).

TABLE IV
CALCULATION AND MEASUREMENTS OF THE OVERALL SYSTEM EFFICIENCY

	# of levels	voltage distribution	converter efficiency	linear reg. efficiency	overall efficiency	phases needed
calculation	2	0.5Vmax/Vmax	93.27	64.52	60.18	2
calculation	3	0.33Vmax/0.67Vmax/1Vmax	90.01	71.7	64.54	3
calculation	3	0.5Vmax/0.75Vmax/1Vmax	86.55	73.59	63.69	4
measurement	3	0.5Vmax/0.75Vmax/1Vmax	85	75.21	64.03	4
calculation	4	0.25Vmax/0.5Vmax/0.75Vmax/Vmax	86.29	76.93	66.39	4
measurement	4	0.25Vmax/0.5Vmax/0.75Vmax/Vmax	84.81	77.9	67.38	4
calculation	5	0.2Vmax/0.4Vmax/0.6Vmax/0.8Vmax/Vmax	82.74	80.05	66.23	5

The switching frequency of the transformer coupled converter is 2 MHz. Voltage distribution is scaled with vmax, hence 0.5 V_{max}/V_{max} corresponds to voltage levels of 8.5V and 17 V when V_{max} is 17 V.

In this implementation of envelope amplifier, the efficiency drop in the multilevel converter (from 90% to 86.6% with IRF8915 MOSFET) is more predominant than the efficiency boost of the linear regulator (obtained by proper selection of the voltage levels, from 71.7% to 73.6%). Therefore, the power losses are better optimized when the multilevel voltage distribution is performed at high voltage levels. In these cases, three equidistant voltage levels (0.33Vmax/0.67Vmax/Vmax) are more appropriate considering the whole system efficiency (transformer-coupled converter + linear regulator). The best overall efficiency, for the considered design, is obtained with four phases and four voltage levels.

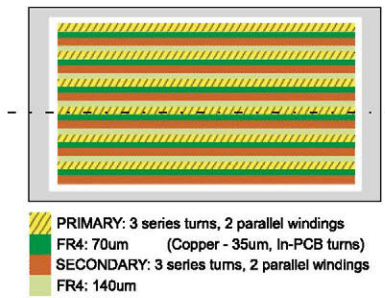


Fig. 18. Transformer is implemented in a 12-layer PCB, primary and secondary windings are interleaved. With this construction, the transformer is symmetrical.

IV. APPLICATION EXAMPLE: ENVELOPE POWER SUPPLY FOR THE RF AMPLIFIER

This section is divided into two parts. First, a transformer-coupled converter is designed for following a sinusoidal envelope reference; the converter is implemented and duty cycle steps are applied to this converter. Second, this converter, with a different setup, is used to implement the EER solution presented in [2]. Experimental measurements are given for both implementations.

A. Design for Sinusoidal ET

An experimental prototype is built as shown in Fig. 12(a), with the following specifications: 24 V input voltage, four phases (duty cycles of 0%, 25%, 50%, 75%, and 100% are available), the input capacitor is formed by $4x22\ \mu$F multiLayer ceramic capacitors (MLCC), the output capacitor is 47 nF MLCC, maximum output power is $P_{\mathrm{OUTMAX}} = 30$ W. The converter is implemented in a 12-layer PCB and the windings of the transformers are integrated in the PCB; the construction of the four transformers is identical, it is shown in Fig. 18. Measurements for the magnetizing and leakage inductances are shown in Table V. Total series inductance L_{SERIES} is estimated in 30 nH, the implemented prototype can be operated at 4 MHz and 2 MHz switching frequency.

Duty cycle changes are scheduled in the control of the converter (a Spartan III board) according to a sinusoidal signal. These duty cycles are scheduled taking into account that three levels are available and that nonequidistant voltage distribution (0.5 Vmax/0.75 Vmax/Vmax with $V\mathrm{max} = 24$) is used. The duty cycle is changed according to the following criteria:

TABLE V
INDUCTANCE MEASUREMENTS OF THE TRANSFORMERS

	Leakage Inductance	Magnetizing Inductance
Transformer 1	$21nH$	$9.2\mu H$
Transformer 2	$20nH$	$10.1\mu H$
Transformer 3	$19nH$	$9.4\mu H$
Transformer 4	$22nH$	$8.8\mu H$

Measurements are done at Mhz.

1) when the amplitude of the sinusoidal envelope reference is between 75% and 100%, the duty cycle of the converter is $d = 100\%$;
2) when the amplitude of the sinusoidal envelope reference is between 50% and 75%, the duty cycle of the converter is $d = 75\%$;
3) when the amplitude of the sinusoidal envelope reference is between 0% and 50%, the duty cycle of the converter is $d = 50\%$.

The switching frequency of the envelope reference is 170 kHz and the sampling ratio N_S is set to 14 as shown in Fig. 13(a). According to (6), the operating frequency of the transformer-coupled converter should be 2 MHz in order to follow this envelope reference. The measurement of the resulting output voltage is shown in Fig. 19.

When the transformer coupled converter is operated at 4 MHz switching frequency, it is able to follow a sinusoidal envelope reference of 350 kHz; this is illustrated in Fig. 19.

For these measurements, the converter is operated in open loop and with a 10 Ω load. The ripple at the output voltage of the converter (see Figs. 19 and 20) appears because during the switching of the MOSFETs the sum of the input voltage

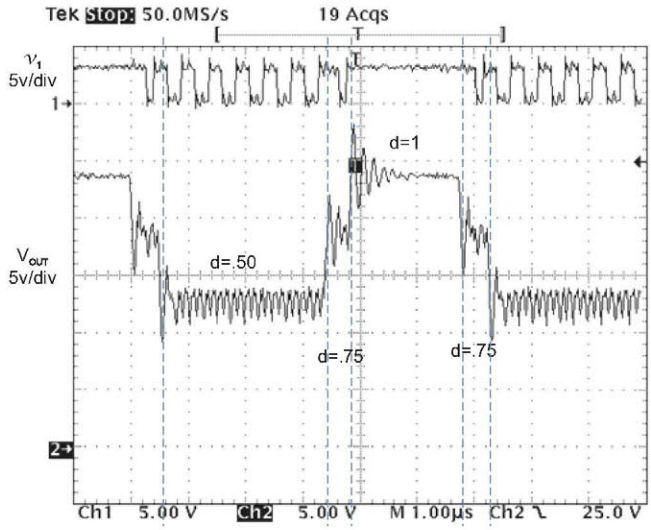


Fig. 19. Output voltage waveform of the converter for $f_{SW} = 2$ MHz and an output capacitor of 47 nF. The frequency of the sinusoidal envelope reference that modulates the duty cycle is 170 kHz. v_1 is the voltage of phase 1 (see Fig. 7). V_{OUT} is the output voltage of the converter.

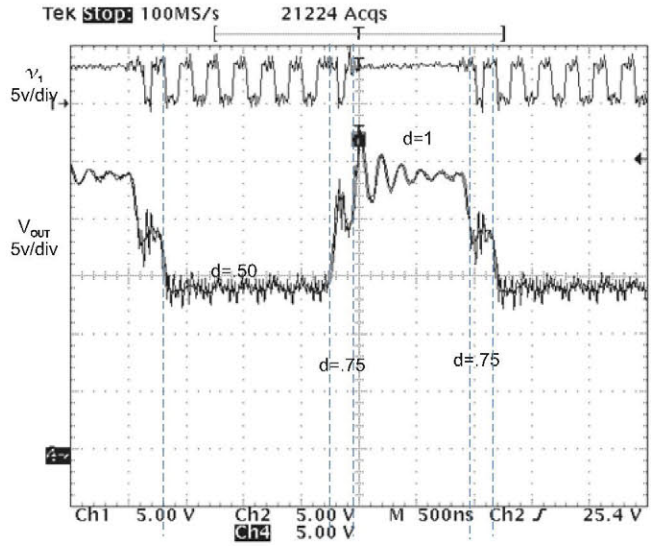
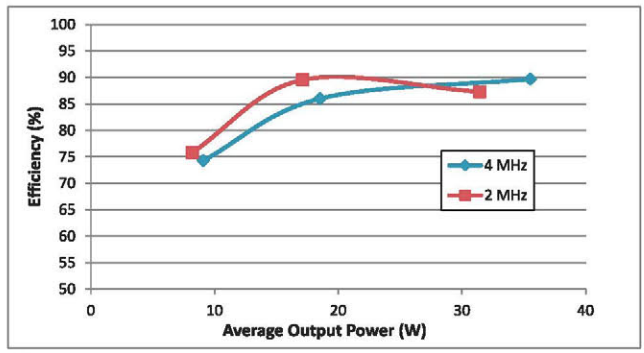


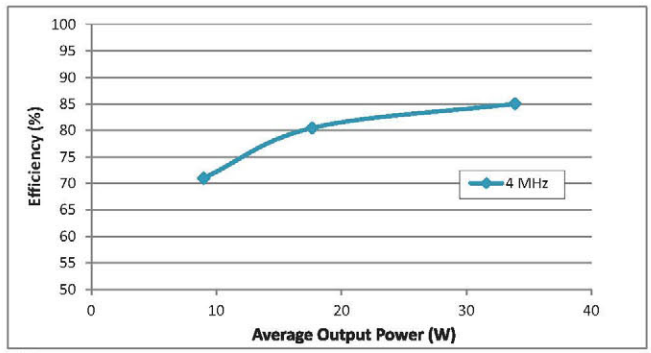
Fig. 20. Output voltage waveform of the converter for $f_{SW} = 4$ MHz and an output capacitor of 47 nF. The frequency of the sinusoidal envelope reference that modulates the duty cycle is 350 kHz. v_1 represents the voltage of phase 1 (see Fig. 7). V_{OUT} is the output voltage of the converter.

to the magnetic structure is not kept constant, this ripple can be reduced to some extent by changing the dead times between main MOSFETs of different phases and between main MOSFET and synchronous rectifier MOSFET. This is explained in detail in [8].

Efficiency measurements are done for both aforementioned conditions: the efficiency of the transformer-coupled converter following a 170 kHz sinusoidal envelope reference is shown in Fig. 21(a) for operating frequencies of 2 and 4 MHz; the efficiency of the converter following a 350 kHz sinusoidal envelope reference is shown in Fig. 21(b) for operating frequency



(a)



(b)

Fig. 21. Efficiency measurements of the experimental prototype for frequencies of 2 MHz and 4 MHz, following sinusoidal envelope references of 170 kHz and 350 kHz. Different load resistances are used for these measurements, 40 Ω, 20 Ω, and 10 Ω.

TABLE VI
SUMMARY OF EFFICIENCY MEASUREMENTS FOR THE TRANSFORMER-COUPLED CONVERTER AT 2 MHZ AND 4 MHZ SWITCHING FREQUENCY WITH DIFFERENT ENVELOPE REFERENCES

envelope reference amplitude	envelope reference frequency	converter frequency	converter efficiency
$0V$ - $24V$	$170kHz$	$2MHz$	87%
$0V$ - $24V$	$170kHz$	$4MHz$	90%
$0V$ - $24V$	$350kHz$	$4MHz$	85%

Measurements are reported for 10 Ω load.

of 4 MHz. For these operating conditions, the efficiency is measured for different load resistances (10 Ω, 20 Ω, and 40 Ω); the corresponding average output power is shown in the horizontal axis. A summary of the efficiencies obtained for a load resistance of 10 Ω is shown in Table VI.

B. Complete System Setup

The envelope amplifier shown in Fig. 11 is implemented. The transformer-coupled converter is placed in series with a linear regulator. In this linear regulator, the MOSFET and an operational amplifier suitable for high frequency are chosen. The LM6172 operational amplifier is selected. It is a wide bandwidth operational amplifier with an open loop bandwidth of 100 MHz. The input capacitance of the MOSFET should be as low as possible; hence, the HF/VHF power MOS transistor is selected. The input capacitance of the HF/VHF transistors is in the order of the hundreds of pF; another reason for the selection of low input capacitance is due to the control of the MOSFET.

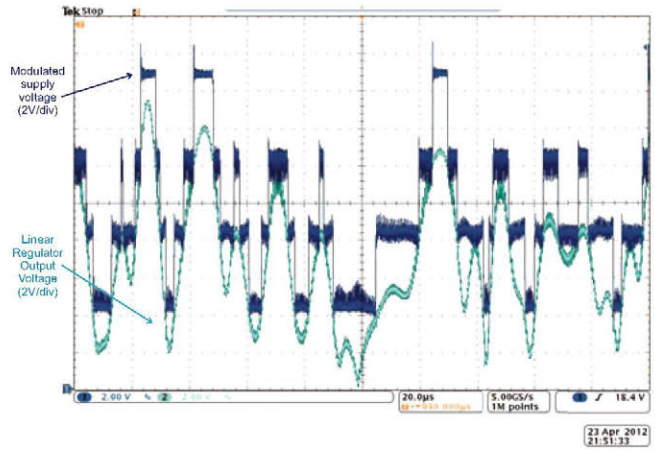


Fig. 22. Experimental measurement of an envelope amplifier implemented with the transformer coupled converter and following a 200 kHz 64QAM signal with four levels. Modulated supply voltage waveform is shown in 2 V/div scale, output voltage of the linear regulator is 2V/div and time scale is 20 μs/div.

It is controlled directly from the output of the operational amplifier and, therefore, the lower the capacitance between MOSFET's gate and source, the better, because a high capacitance can lead to the current saturation of the operational amplifier's output. High transconductance is also important because it actually represents the voltage that should be applied between the MOSFET's gate and source. Several MOSFETs from BLF series have been tested, and due to its good overall characteristics, BLF 177 has been selected.

The setup of the transformer-coupled converter is as follows: the same 12-layer PCB has been used with IRF8915 MOSFETs and LM27222 drivers; the operating frequency is 2 MHz. The system is tested with a 200 kHz 64QAM signal with a maximum amplitude of 16 V. The average output power of this signal is around 10.5 W while the peak power is 50 W. A relevant time diagram of the linear regulator and the multilevel converter is shown in Fig. 22.

V. Conclusion

In this paper, a PWM multiphase topology based on transformer-coupling is proposed for voltage modulation techniques in RF architectures. In this multiphase topology, the coupling between phases is done by using transformers instead of coupling inductors. Since transformers are, ideally, no energy storage devices, the transfer of energy from the input to the output of the converter is done very fast, which allows a fast change in the output voltage.

With no energy storage in the converter, the dynamic response does not depend on the switching frequency; hence, the operating frequency of the converter can be chosen according to the dynamic of the envelope reference (in the case of RF applications), or load dynamics (in the case of DVS).

Following this guideline, a demonstrator, where the duty cycle is modulated with a 170 kHz sinusoidal waveform has been presented, showing good efficiency (see Table VI) and a correct tracking of the modulating waveform. The presented prototype running at 4 MHz is able to properly follow 170 kHz and 350 kHz envelope references with a three-level resolution.

A theoretical analysis of the overall envelope amplifier efficiency is presented. Conditions for choosing the number of levels and the voltage distribution for maximum efficiency are derived for the presented envelope amplifier.

An implementation of the envelope amplifier proposed in [2] is done using the transformer-coupled converter. In this implementation, a 200-kHz 64QAM signal is followed with a 2-MHz converter; experimental measurements are given; the efficiency is 84.8% in the transformer-coupled converter, 77.9% in the linear regulator, and 67.4% for the overall envelope amplifier.

From this implementation, it can be concluded that the transformer-coupled converter is an interesting candidate for the implementation of voltage modulation techniques thanks to its efficiency and fast transient response.

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